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10/772,590	02/04/2004	Roberto Pelliconi	61181-00011USPX	2338

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EXAMINER	
PUENTE, EVA Y	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,590	PELLICONI ET AL.	
	Examiner	Art Unit	
	EVA Y. PUENTE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-12,14,16,17,19 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3, and 25* is/are allowed.

6)☒ Claim(s) *4,6,8-12,19 and 21-23* is/are rejected.

7)☒ Claim(s) *5,7,14,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Amendment, filed 2/28/08, with respect to the rejection(s) of claim(s) 2-12, 14, 16-17, 19, 21-24, and 25 under have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

Claim Objections

2. Claim 8 is objected to because of the following informalities: on line 6, please add -- block -- after "first".

3. Claim 14 is objected to because of the following informalities: on line 2, please add -- and -- after "signal"; on line 10, please add -- entity -- after "transmitting", on line 10, please add -- to -- after "over".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 4, 8, 22, and 23 are rejected under 35 U.S.C. 102(e) as being unpatentable by Hirose et al (US 6,917,995).

a) Regarding claim 4, Hirose et al disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit (IC; abstract) comprising a transmitter block (block A in Fig. 1A) and a receiver block (block B in Fig. 1A) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (command bus line in Fig. 1A);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (CMD_READY_B bus line control the command; Col 4, L36-64, wherein the issuable stages inherent as no congestion in the second block);

generating on a third line a synchro signal starting from said transmitter block (STRB_A bus line), this synchro signal indicating to the receiver block that the data signal comprises a new datum (Command data line is transmitted continuously), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Col 22, L31-33; command issuing control circuit 12 in Fig. 2A controls Command data line and STRB_A bus line in Fig. 5A); and

reading, by the receiver block, of the data signal with a different sampling period than the transmission period of the transmitter block (it is inherent that device A and device B are generated with different clock signals).

b) Regarding to claim 8, Hirose et al disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit (IC; abstract) comprising a first block (block A in Fig. 1A) and a second block (block B in Fig. 1A) connected through a communication network, comprising:

generating a data signal having a transmission period on a first bi-directional line that from said first block must be received by the second block (command bus line 10 in Fig. 5A);

generating on a second line a congestion signal from the second block to the first block when a congestion event of the second block occurs in order to interrupt the transmission of said data signal (CMD_READY_B bus line control the command; Col 4, L36-64, wherein the issuable stages inherent as no congestion in the second block);

generating on a third line a synchro signal starting from said first block (STRB_A bus line), this synchro signal indicating to the second block that the data signal comprises a new datum (Command data line is transmitted continuously), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the second block occurs (Col 22, L31-33; command issuing control circuit 12 in Fig. 2A controls Command data line and STRB_A bus line in Fig. 5A); and

generating, on a couple of further line, a couple of unidirectional signals indicating the transmission direction on the first bi-directional line between said first block and said second block (CMD_READY_A, STRB_B), a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the second block (REQUEST, GRANT).

c) Regarding to claim 22, Hirose et al disclose a communication system, comprising:

a first communication block (block A in Fig. 1A);

a second communication block (block B in Fig. 1A);

a communication network interconnecting the first and second communication blocks (Fig. 1A); the communication network comprising:

a first communication line for carrying a data signal (command bus line in Fig. 1A);

a second communication line for carrying a congestion signal (CMD_READY_B bus line control the command; Col 4, L36-64, wherein the inhibiting command is inherent as congestion condition occurs); and

a third communication line for carrying a synchronization signal (STRB_A bus line Fig. 5A); wherein the synchronization signal is active whenever the data signal on the first communication is new datum and inactive whenever the congestion signal on the second communication line is active (command issuing control circuit 12 in Fig. 2A controls Command data line and STRB_A bus line in Fig. 5A);

wherein the first, second and third communication lines are bi-directional, further including:

a transmit signal line (GRANT in Fig. 5A); and

a receive signal line (REQUEST in Fig. 5A);

wherein the transmit and receiver signal lines interconnected the first and second communication blocks (block A and B), and control signals thereon specify, for the bi-

directional first communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal (REQUEST, GRANT controls communication between block A and B).

d) Regarding to claim 23, Hirose et al disclose a request signal line that interconnects the first and second communication, and a control signal thereon used to negotiate which of the first and second communication blocks is to be transmitter/receiver (REQUEST, GRANT in Fig. 5A controls communication between block A and B).

6. Claims 4, 8, 22, and 23 are rejected under 35 U.S.C. 102(e) as being unpatentable by Upp (US 5,901,146).

a) Regarding claim 4, Upp discloses a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block (bus master 100 in Fig. 5) and a receiver block (user 112) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (Data on bus 118);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (CONJ bus 128);

generating on a third line a synchro signal starting from said transmitter block (FRAME bus line), this synchro signal indicating to the receiver block that the data

signal comprises a new datum (new data is inherent since data line is bi-directional and transmitted continuously), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Col 6, L25-49); and

reading, by the receiver block, of the data signal with a different sampling period than the transmission period of the transmitter block (it is inherent that device A and device B are generated with different clock signals. The data is transferred between asynchronous devices).

b) Regarding to claim 8, Upp disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a first block (bus master 100 in Fig. 5) and a second block (user 112) connected through a communication network, comprising:

generating a data signal having a transmission period on a first bi-directional line that from said first block must be received by the second block (Data on bus 118);

generating on a second line a congestion signal from the second block to the first block when a congestion event of the second block occurs in order to interrupt the transmission of said data signal (CONJ bus 128; Col 6, L44-59);

generating on a third line a synchro signal starting from said first block (FRAME bus line), this synchro signal indicating to the second block that the data signal comprises a new datum (new data is inherent since data line is bi-directional and transmitted continuously), and in that the congestion signal interrupts also the

transmission of said synchro signal when a congestion event of the second block occurs (Col 6, L44-59); and

generating, on a couple of further line, a couple of unidirectional signals indicating the transmission direction on the first bi-directional line between said first block and said second block (CLOCK bus line, ACK bus line 126), a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the second block (Col 6, L36-44).

c) Regarding to claim 22, Upp disclose a communication system, comprising:

a first communication block (bus master 100 in Fig. 5);

a second communication block (user 112);

a communication network interconnecting the first and second communication blocks (bus lines as shown in Fig. 5); the communication network comprising:

a first communication line for carrying a data signal (Data on bus 118);

a second communication line for carrying a congestion signal (CONJ bus 128; Col 6, L44-59); and

a third communication line for carrying a synchronization signal (FRAME bus line); wherein the synchronization signal is active whenever the data signal on the first communication is new datum and inactive whenever the congestion signal on the second communication line is active (Col 9, L29-51);

wherein the first, second and third communication lines are bi-directional (Col 6, L28-31), further including:

a transmit signal line (CLOCK bus line)); and

a receive signal line (ACK bus line);

wherein the transmit and receiver signal lines interconnected the first and second communication blocks, and control signals thereon specify, for the bi-directional first communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal (Col 6, L L36-44).

d) Regarding to claim 23, Upp disclose a request signal line that interconnects the first and second communication, and a control signal thereon used to negotiate which of the first and second communication blocks is to be transmitter/receiver (Col 6, L L36-44).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6, 9, 10, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable by Hirose et al (US 6,917,995) in view of Applicant Admitted Prior Art (AAPA).

a) Regarding to claim 6, Hirose et al disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit (IC; abstract)

comprising a transmitter block (block A in Fig. 1A) and a receiver block (block B in Fig. 1A) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (command bus line in Fig. 1A);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (when number of commands reach maximum limit) of the receiver block occurs in order to interrupt the transmission of said data signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

generating on a third line a synchro signal starting from said transmitter block (STRB bus line in Fig. 1A), this synchro signal indicating to the receiver block that the data signal comprises a new datum (Fig. 1B; Col 1, L60-65), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Fig. 1B; Col 1, L63-Col 2, L6; STRB signal stops after the BUSY signal is sent).

Hirose et al disclose all the subject matters above except for the specific teaching that the first, second and third communication lines are each comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1----Bn in Fig. 1). The tristate type of repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion communication line (6a) drive the tristate operation of the repeater devices for the data

communication line in response to the congestion signal. These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of repeaters in communication line of AAPA with the data transfer system of Hirose et al. By doing so, provide better signal sampling and maintain voltage level of signals.

b) Regarding to claim 9, Hirose et al disclose an integrated electronic circuit being integrated on a semiconductor substrate (IC; abstract) comprising a transmitter block (block A in Fig. 1A) and a receiver block (block B in Fig. 1A) connected through a communication network, said communication network comprising a first line for a data signal (command bus line in Fig. 1A), a second line for a congestion signal (BUSY bus line in Fig. 1A; Col 1, L52-59), and a third line for a synchro signal (Fig. 1B; Col 1, L63-Col 2, L6; STRB signal stops after the BUSY signal is sent).

Hirose et al disclose all the subject matters above except for the specific teaching that the first, second and third communication lines are each comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1----Bn in Fig. 1). The tristate type of repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion communication line (6a) drive the tristate operation of the repeater devices for the data communication line in response to the congestion signal. These repeaters are capable

of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of repeaters in communication line of AAPA with the data transfer system of Hirose et al. By doing so, provide better signal sampling and maintain voltage level of signals.

c) Regarding to claim 10, Hirose et al disclose wherein said signal line comprises a couple of further lines for unidirectional signals indicating the transmission direction between said transmitter block and said receiver block (Fig. 2A and 2C), a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the receiver block (counter 18, controller A, counter 18B, controller B constitutes as negotiator).

d) Regarding to claim 19, Hirose et al disclose a communication system, comprising:

a first communication block (block A in Fig. 1A);

a second communication block (block B in Fig. 1A);

a communication network interconnecting the first and second communication blocks (Fig. 1A); the communication network comprising:

a first communication line for carrying a data signal (command bus line in Fig. 1A);

a second communication line for carrying a congestion signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

a third communication line for carrying a synchronization signal (STRB bus line in Fig. 1A); wherein the synchronization signal is active whenever the data signal on the first communication is new datum and inactive whenever the congestion signal on the second communication line is active (Fig. 1B; STRB signal is active as the command signal is new and within process limit, while STRB stops transmitting when BUSY is active after limit of commands has reached).

Hirose et al disclose all the subject matters above except for the specific teaching that the first, second and third communication line is each split into corresponding stages and comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1--Bn in Fig. 1). These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of repeaters in communication line of AAPA with the data transfer system of Hirose et al. By doing so, provide better signal sampling and maintain voltage level of signals.

e) Regarding to claim 21, AAPA disclose tristate type of repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion communication line (6a) drive the tristate operation of the repeater devices for the data communication line in response to the congestion signal. Therefore, it is obvious to one of ordinary skill in art

to implement the tristate repeater device in the additional communication lines for further improve communication system.

9. Claims 6, 9, 10, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable by Upp (US 5,901,146) in view of Applicant Admitted Prior Art (AAPA).

a) Regarding to claim 6, Upp disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block (100 in Fig. 5) and a receiver block (112 in Fig. 5) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (Data bus line 118);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (CONJ bus line 128; Col 6, L44-49); and

generating on a third line a synchro signal starting from said transmitter block (FRAME bus line), this synchro signal indicating to the receiver block that the data signal comprises a new datum (it is inherent since Data bus line is bi-directional and transmit continuously), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Col 6, L L44-49).

Upp disclose all the subject matters above except for the specific teaching that the first, second and third communication lines are each comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1-Bn in Fig. 1). The tristate type of repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion communication line (6a) drive the tristate operation of the repeater devices for the data communication line in response to the congestion signal. These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of repeaters in communication line of AAPA with the data transfer system of Upp. By doing so, provide better signal sampling and maintain voltage level of signals.

b) Regarding to claim 9, Upp disclose an integrated electronic circuit being integrated on a semiconductor substrate comprising a transmitter block (100 in Fig. 5) and a receiver block (112 in Fig. 5) connected through a communication network, said communication network comprising a first line for a data signal (Data bus line 118), a second line for a congestion signal (CONJ bus line 128; Col 6, L44-49), and a third line for a synchro signal (FRAME bus line).

Upp disclose all the subject matters above except for the specific teaching that the first, second and third communication lines are each comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1-Bn in Fig. 1). The tristate type of repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion

communication line (6a) drive the tristate operation of the repeater devices for the data communication line in response to the congestion signal. These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of repeaters in communication line of AAPA with the data transfer system of Upp. By doing so, provide better signal sampling and maintain voltage level of signals.

c) Regarding to claim 10, Upp disclose wherein said signal line comprises a couple of further lines for unidirectional signals indicating the transmission direction between said transmitter block and said receiver block (100 and 112 in Fig. 5), a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the receiver block (ACK bus line 126; Col 6, L37-44).

d) Regarding to claim 19, Upp disclose a communication system, comprising:

a first communication block (100 in Fig. 5);

a second communication block (112 in Fig. 5);

a communication network interconnecting the first and second communication blocks (bus lines in Fig. 5); the communication network comprising:

a first communication line for carrying a data signal (Data bus line 118);

a second communication line for carrying a congestion signal (CONJ bus line 128; Col 6, L44-49); and

a third communication line for carrying a synchronization signal (FRAME bus line); wherein the synchronization signal is active whenever the data signal on the first

communication is new datum and inactive whenever the congestion signal on the second communication line is active (Col 9, L29-51).

Upp disclose all the subject matters above except for the specific teaching that the first, second and third communication line is each split into corresponding stages and comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1-Bn in Fig. 1). These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of repeaters in communication line of AAPA with the data transfer system of Upp. By doing so, provide better signal sampling and maintain voltage level of signals.

e) Regarding to claim 21, AAPA disclose tristate type of repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion communication line (6a) drive the tristate operation of the repeater devices for the data communication line in response to the congestion signal. Therefore, it is obvious to one of ordinary skill in art to implement the tristate repeater device in the additional communication lines for further improve communication system.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable by Applicant Admitted Prior Art (AAPA).

a) Regarding to claim 11, AAPA discloses an architecture for manufacturing an integrated electronic circuit being integrated on a semiconductor substrate comprising a transmitter block (2a in Fig. 1) and a receiver block (3a) connected through a communication network, said communication network comprising a plurality of signal lines each split in elementary blocks (An), each block being separated through a repeater (Bn), said elementary blocks being connected to said receiver and transmitter blocks through interface devices equipped with unidirectional signals ([0015-0018]), wherein each elementary block (An) is realized through a crossbar multiplexer ([0063]). AAPA discloses crossbar multiplexers are used in conventional network for connecting two points. AAPA did not specify the multiplexer is 2x2.

However, such limitation is matter of design choice. The size of the switch does not change operation property and operation result, so long the network produces secure and reliable switching. Therefore, it is obvious to one of ordinary skill in the art to implement 2x2 multiplexer for faster switching operation in the network communication device.

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable by Applicant Admitted Prior Art (AAPA) in view of Hirose et al (US 6,917,995).

a) Regarding claim 12, AAPA disclose all the subject matters above except for the specific teaching of a negotiation between the transmitter and receiver block. However, Hirose et al disclose data transfers between two integrated circuit devices (Fig. 5A), wherein comprise a bi-directional command data line (10), CMD_READY_A, CMD_READY_B, REQUEST, and GRANT (negotiation) to define the transmission

direction between integrated circuit A and B (Col 7, L28-58). This way avoid data collision and provides accurate data communication between two devices. Therefore, it is obvious to one of ordinary skill in the art to combine the data control of Hirose et al with the IC communication system of AAPA. By doing so, provide efficient bus and data control in IC system.

12. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable by Applicant Admitted Prior Art (AAPA) in view of Upp (US 5,901,146).

a) Regarding claim 12, AAPA disclose all the subject matters above except for the specific teaching of a negotiation between the transmitter and receiver block. However, Upp disclose data transfers between two communication devices (100 and 112 Fig. 5), wherein comprise a bi-directional command data line (118), ACK 126, CONJ 128 to define the transmission direction between integrated circuit A and B (Col 6, 25-49). This way to avoid data collision and provides accurate data communication between two devices. Therefore, it is obvious to one of ordinary skill in the art to combine the data control of Upp with the IC communication system of AAPA. By doing so, provide efficient bus and data control in IC system.

Allowable Subject Matter

13. Claims 2-3 and 25 are allowed.

14. Claims 5 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is an examiner's statement of reasons for allowance: None of the prior art teaches or suggests data communication system between two integrated circuit comprises a synchro signal on a bus line, wherein the synchro signal is delayed with respect to the data signal which is communicated over a first bus line. The synchro signal indicates to the second integrated circuit that the data signal on the first line comprises a new datum.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Puente whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Puente
/E. Y. P./
Examiner, Art Unit 2611

July 2, 2008

/Chieh M. Fan/
Supervisory Patent Examiner, Art Unit 2611